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# A Review on XOR-Free Approach for Implementation of Convolutional Encoder

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**Abstract**: Due to the excellent error control performance in many communication systems Convolution encoder and Viterbi decoder are widely used. In coding techniques the number of symbols in the source encoded message is increased in a controlled manner in order to facilitate two basic demand at the receiver one is Error detection and other is Error correction. The amount of error detection and correction required and its efficiency depends on the signal to noise ratio (SNR). The technology based on Non Line of Sight (NLOS) ability to make the system very attractive for users, but there will be a little higher BER at low SNR. Coding is a technique where redundancy is added to original bit sequence to increase the reliability of the communication. This paper presents a review on hardware implementation of Convolution Encoder with power efficient architecture. The results of this architecture will decrease the dynamic power and HW cost with lower design complexity as comparing to conventional method.

**Keywords**: Automatic Repeat Request (ARQ), Forward Error Correction (FEC), Convolutional Code (CC), Non Line of Sight (NLOS).

## I. INTRODUCTION

In a communication system, error detection and correction mechanisms are vital and numerous techniques exist for reducing the consequence of bit-errors and trying to make sure that the receiver eventually gets an error free version of the packet. The most important technique used are fault detection with Automatic Repeat Request (ARQ), Forward Error Correction (FEC) and hybrid forms of ARQ and FEC. This development focus on FEC techniques. Forward Error Correction (FEC) is an error control method for data transmission by adding redundant data to its messages to improve the capacity of a channel. This redundant data allows the receiver to detect and to correct a certain number of errors without asking the encoder to re-transmit more additional data. The process of adding this redundant information is known as channel coding. Mainly there are two major kinds of channel coding: block codes like Reed –Solomon coding and Convolution coding. Block codes work with fixed length blocks of code. Convolution codes deal with data sequentially. Block codes become very complex as their length increases and are therefore harder to implement. Convolution codes in comparison to block codes are less complex and therefore easier to implement.

### Convolutional Code (CC)

In Non Line of Sight (NLOS) Communication such as Mobile Wi-Max of CDMA part, the CC is the only required coding scheme. Its computations depend not only on the existing set of input symbols it also depends up on some of the previous used input symbols. A lattice description is used for convolution encoding that show relation how each possible input to the encoder impacts on the output in shift register.Viterbi algorithmis used for decoding. In communication, a convolution code is a type of error-correcting code in which Each m-bit information symbol (each m-bit string) to be encoded is transformed into an n-bit symbol, where m/n is the code rate (n ≥ m). The transformation is a function of the last information symbols, where k is the constraint length of the code.

The convolutional codes are defined by three parameters which are as follow:

(a) Rate: Ratio of the number of input bits to the number of output bits. In this example, rate is 1/2 which means there are two output bits for each input bit.

(b) Constraint length: The number of delay elements in the convolution coding for example with k = 3 , there are two delaying elements.

c) Generator polynomial: Wiring of the input sequence with the delay elements to form the output. For example, generator polynomial is [7,5]8 = [111,101]2 . The output from the 78 = 1112 arm uses the XOR of the current input, previous input and the previous to previous input. The output from 58 = 1012 uses the XOR of the current input and the previous to previous input.

Rate = ½
Constrain length, k=3
Generator polynomial is $[7, 5]_8 = [111,101]_2$

**Generic Methods for Decoding Convolution code**

There are many different decoding techniques for Convolution codes which are Feedback decoding, sequential decoding and maximum prospected decoding.

1. Threshold decoding – This decoding is called majority logic decoding. It is successfully applied only on definite classes of code. It applies to channel having a slight to good SNR. It is far away from optimal because of its inferior in bit error performance.

2. Sequential decoding –This decoding is sub optimal. This decoding has better performance than the previously used method. Virtually independent from the length of the particular code is the advantage of it. Unpredictable decoding latency & variable decoding time is its drawback. Also, it requires a large memory.

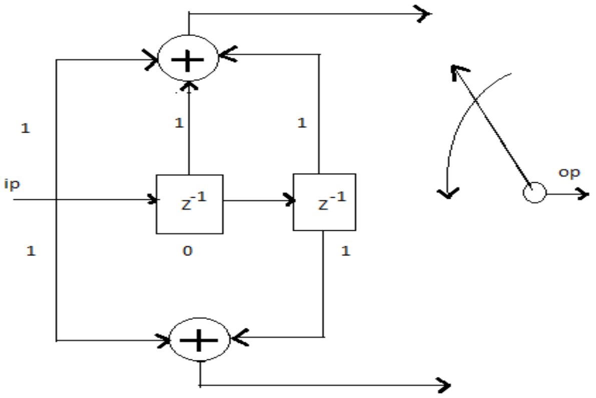


Figure 1: Convolutional code with Rate 1/2, K=3, Generator Polynomial octal

3. Viterbi decoding - It is optimal algorithm for decoding of Convolution code. It is the dominant technique for Convolution codes. It has advantages like satisfactory bit error performance, low cost, fixed decoding time.

The most extensively decoding algorithms for Convolution codes is Viterbi code proposed in 1967. It is very useful method for forward error correction. In many wireless communication systems like IEEE 802.11a/g, Wi-Max, WCDMA and GSM to improve capacity of communication channel it is widely used. Due to high demand of the portable wireless communication devices by user. So need of high speed viterbi decoder increasing.

## II. LITERATURE SURVEY

G. Purohit, et. al. [1] "A New XOR-Free Approach for Implementation of Convolutional Encoder" In this projected work a brand new algorithmic rule to construct an XOR-Free architecture of an influence efficient Convolutional Encoder. optimisation of XOR operators is that the main concern whereas implementing polynomials over GF(2), that consumes a significant quantity of dynamic power. The projected approach utterly removes the XOR-processing operation of a selected non systematic, feed-forward generator polynomial and reduces the logical operators, thereby the encoding value. Hardware (HW) implementation of the projected design uses ROM (ROM) with pre processed addressing operations to reduce read-only memory size by nearly five hundredth. The results of the new architecture reduce the dynamic power up to 21.4% and HW cost up to 15% with lesser design complexity as compared to conventional method. The Hardware co simulation of the architecture is first validated and then implemented with Xilinx Virtex-V FPGA. The problem of optimization of modulo-2 adder and proposes a novel algorithm to implement XOR-Free architecture for Convolutional Encoder. The approach reduces the standard polynomial into a ROM and eases the FPGA implementation. The architecture is successfully tested for 3GPP and 3GPP2 wireless standards.

John Dielissen et.al. [2] "Multi standard FEC Decoders for Wireless Devices" In this proposed work is based on the compression of the era of mobile terminal the real-time support of multiple/different transmission standards. Forward error correction decoding functionality is including in some of these standards. Author review the options for the arrangements of common decoder families (Reed–Solomon, Viterbi, Turbo and low-density parity check) within same hardware platform. That although desired combinations may result in silicon area saving, in general cases the reuse possibilities are limited to much less than the overall decoder area. Due to the need of handy and fast processing area reduction and low power consuming devices are widely used.

Joachim Hagenauer et.al. [3] "Forward error correcting for CDMA systems" In this proposed work the technique or principle is based on Spread spectrum systems, forward error correcting (FEC) methods is applied in specially code division multiple access systems (CDMA). In fact, almost all CDMA systems use one or the other way of FEC. Author covering some aspect of FEC channel coding in CDMA system: CDMA/FEC system viewed as concatenated schemes with inner and outer decoding. And how such a system can be improved by using a soft-in/soft-out decoder which passes a soft decision from the inner to the outer decoder. Further improvement is gained by using another soft-in/soft- out decoder for the outer code.

A. J. Viterbi et. al. [4] "Convolutional codes and their performance in communication systems" In this proposed work on, At present time, many applications such as telephonic conversations that need communication in which the messages are encoded into the communication channel and then decoding it at the receiver end. When message transferring, the data may get corrupted because of noise in the communication channel. So decoder tool have capability of correcting the error.

Viterbi algorithm has got many applications due to its error detection and correction nature. Convolution encoding with Viterbi decoding is a common way for forward error correction. Due to the limited capacity of the communication channels. It has been widely deployed in many wireless communication systems.

Y.Yibin et.al. [5] "Power consumption in XOR based circuits" In this proposed work XOR gates has advantages in modern circuit design, e.g. smaller size and better testability. That consider power consumption in XOR dominated circuits and evaluate such designs with usual AND/OR logic. We probe the suitability of using different delay models like fan-out delay, unit delay and random delay in XOR dominated logic. Due to (charging and discharging) internal node capacitances is also considered as the Power losses.

R. Pasko et.al. [6] "A new algorithm for elimination of common sub-expressions" In this proposed method An efficient hardware implementation of multiplications with one or more constant is faced in various digital signal-processing areas, such as reflection dispensation or digital filter optimization is a problem. The solution of this is to design low power design.So targeting on the parameter area and power efficient hardware implementation.

## III. METHOD

Viterbi algorithm is the most possibility decode algorithm of convolution code. Viterbi decoder means the VLSI implementation of Viterbi algorithm. In the area of communication, convolution code is very popular, so how to improve the performance and reduce the power and area of the decoder is important. In the other hand, different protocols use different convolution code and varied applications have different requirement for throughput, area and power. So design of reusable Viterbi decoder is important, too. This decoder adopted the Process Element (PE) technique, which made it easy to adjust the throughput of the decoder by growing or falling the number of PE. By the method of Same Address Write Back (SAWB), we compact the number of register to half in disparity with the method of ping-pong. This decoder supported punctured convolution code and was data-driven, which means the circuit was able to work under different data rate and avoid those invalid operations.PE Process Element, was one of the most popular architecture in digital signal processing .The PE architecture of Viterbi decoder has been introduced. Fig1 is the basic structure of PE in Viterbi decoder. Which consists of PMU, ACSU, BMU and LRU?

Convolution operation is realized using a deterministic finite state machine (DFSM). Its hardware implementation requires a combinational circuit and memory elements. The discrete convolution for the encoded sequence ( $C_j$) can be expressed in terms of information sequence ($I_j$ ) with the generator sequences ($G_I$ ) by the following equation:

$$C_j = \sum_{I=0}^{M} I_{j-I} G_I \qquad (1)$$

Further shift register (SR) based realization of (1) for encoded sequence ($C_{j\beta}$ ) depends upon the length (L) of SR, the present input Ij and M previous input blocks [$I_{j1,\ldots\ldots,} I_{j-M}$] to yield (2)

$$C_{j\beta} = \sum_{\alpha=1}^{n} [\sum_{I=0}^{M} I_{j=I} \alpha g_{\alpha\beta}^{(I)}] \qquad (2)$$

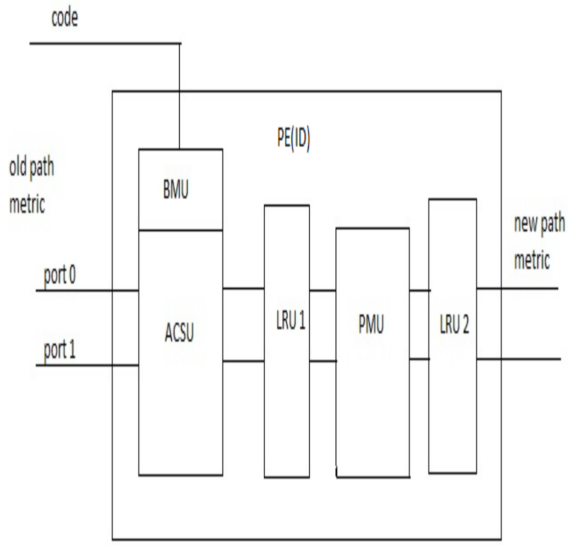


Figure 2: Structure of PE

## IV. CONCLUSION

The improvement in delay can be done by the use of Convolution encoder vedic multiplier. Which provide faster speed than the normal convolution encoder? Parallel generation of partial products and eliminates unwanted multiplication steps by this. A fast multiplication process and achieves a significantly less computational complexity over its conventional counterparts is allow by this algorithm.Viterbi decoder using parallel processing improves processing speed than normal viterbi decoder because the decoder do not need to wait trace back. It means trace back and decoder can simultaneously work. the design complexity will get reduced for inputs of large number of bits and will a provide faster speed. It will also used to design a PN sequence generator and spread spectrum modulation to improve the utilization of bandwidth.

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